HAVERSTOCK & OWENS LLP
260 Sheridan Avenue, Suite 420
Palo Alto, California 94306
(650) 833-0160

A

BOX NEW PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

Attorney Docket No.: ALSC-00300

NEW APPLICATION TRANSMITTAL

Sir:

Transmitted herewith for filing is the patent application of Inventor: Ritu Shrivastava

Title: **A METHOD OF AND APPARATUS FOR INTEGRATING FLASH EPROM AND SRAM CELLS ON A COMMON SUBSTRATE**

CERTIFICATION UNDER 37 CFR § 1.10

I hereby certify that this New Application and the documents referred to as enclosed herein are being deposited with the United States Postal Service on this date, May 20, 1999, in an envelope bearing "Express Mail Post Office To Addressee" Mailing Label Number EL191268477US addressed to: **PATENT APPLICATION**, Assistant Commissioner for Patents, Washington, D.C. 20231.

Danielle Dalton
(Name of Person Mailing Paper)

Signature

Enclosed are:

1. The papers required for filing date under CFR § 1.53(b):

   16 Pages of Specification (including claims); 12 Sheet(s) of Drawings.
   — Formal
   X Informal

2. X Declaration or Oath
3. X Power of Attorney by Assignee
4. X Assignment of the Invention to Alliance Semiconductor (including Form PTO-1595).
5. Fee Calculation

   — Amendment changing number of claims or deleting multiple dependencies is enclosed.

CLAIMS AS FILED

	Number Filed	Number Extra	Rate	Basic Fee
				$760.00
Total Claims	17 - 20 =	0	$18.00	0.00
Independent Claims	5 - 3 =	2	$78 00	156.00
Multiple Dependent claim(s), if any			$260.00	
			Filing Fee Calculation	$916.00

6. Other Fees

   X Assignment Recordation Fee 40.00

   — Other 0.00

   TOTAL FEES ENCLOSED **$956.00**

7. Payment of Fees

   X Check in the amount of $956.00 ($916.00 Basic Filing Fee plus $40.00 Assignment Recordation Fee) enclosed.

8. X Authorization to Charge Additional Fees

   The Commissioner is hereby authorized to charge any additional fees (or credit any overpayment) associated with this communication and which may be required under 37 CFR § 1.16 or § 1.17 to Account No. 08-1275. **An originally executed duplicate of this transmittal is enclosed for this purpose.**

9. — Information Disclosure Statement
10. X Return Receipt Postcard

Dated: May 20, 1999

By: Jonathan O. Owens
Name: Jonathan O. Owens
Registration No.: 37,902

PATENT
Attorney Docket No.: ALSC-00300

A METHOD OF AND APPARATUS FOR INTEGRATING FLASH EPROM AND SRAM CELLS ON A COMMON SUBSTRATE

FIELD OF THE INVENTION

The present invention generally relates to the field of semiconductor memory structures. More particularly, the present invention relates to a method for integrating a nonvolatile erasable programmable read-only flash memory (flash EPROM) and a static random access memory (SRAM) on a common substrate.

BACKGROUND OF THE INVENTION

Flash EPROMS are non-volatile electrically erasable integrated circuit memory devices. Flash EPROMS utilize hot-electron injection for programming and Fowler-Nordheim tunnelling for erase. A cross-section of a conventional flash EPROM is illustrated in Figure 1. The flash memory cell 10 is typically fabricated in a substrate 20 of p-type silicon with a source region 14 optimized for the erase condition and a drain region 16 optimized for hot-electron programming. The flash memory cell 10 also includes a floating gate 18 and a control gate 12, separated by a thin dielectric 22.

In flash EPROMS, the floating gate 18 is typically programmed by channel hot-electron injection, and erased by Fowler-Nordheim tunnelling. Capacitive coupling, in these stacked gate structures, to the control gate 12, creates the field across the floating gate 18 necessary to accumulate the electrons. In order to maximize the capacitive coupling between the control gate 12 and the floating gate 18, the dielectric 22 separating the two is fabricated with as thin a layer as is possible, and from a material having a high dielectric constant. It is known in the prior art to pattern polysilicon to form the floating gate 18. The dielectric 22 is then formed by creating an insulation film on the floating gate 18. This insulation film is typically created by thermally growing silicon oxide, depositing silicon nitride, and then re-

oxidizing the silicon nitride to create an oxidized-nitride-oxide (ONO) layer. Because the control gate 12 and the floating gate 18 are typically patterned from polysilicon, this dielectric layer 22 is often referred to as the inter-poly dielectric. Similarly, a thin dielectric layer 24 referred to as tunnel oxide, exists between the floating gate 18 and the substrate 20.

Generally, local oxidation of silicon (LOCOS) isolation techniques are used during the fabrication of flash EPROM memory cells. The LOCOS isolation technique is optimal for the isolation of flash EPROM cells due to its high reliability and the high internal voltage levels required by flash EPROM cells. Figure 2 illustrates a cross section of the substrate 20 after a LOCOS isolation step is performed. During this LOCOS isolation step, field oxide regions 25 are formed in the substrate 20, separated by a thin layer of sacrificial oxide 26. The active regions are established by a subsequent ion implantation step through the sacrificial oxide 26 and are used to establish the threshold voltage of the cell. The isolation process is designed to achieve an acceptable field threshold voltage to route high voltages in the periphery, and field oxide thickness that gives rise to high coupling coefficients.

One major limitation of LOCOS isolation techniques is the problem of active area encroachment which occurs during the growth of the field oxide regions 25. As shown in Figure 2, during the period of exposure to the oxidizing ambient, areas of the field oxide regions 25 encroach along the edges, thereby forming a bird's beak shaped transition region 28 of SiO_2 around the edges of the field oxide regions 25. This area is not flat and, accordingly, cannot be used effectively for active devices or isolation. Accordingly, the size of useable regions on the substrate 20 is decreased by the LOCOS isolation process. Furthermore, the LOCOS isolation technique requires a larger amount of space for device packing compared to other isolation techniques.

Present static random access memory (SRAM) devices typically use shallow trench isolation (STI) techniques. This is due to the fact that SRAMs do not require voltage levels as high and endurance requirements as stringent as flash EPROM devices. STI techniques

have a drawback of not being compatible with higher voltages and endurance requirements. However, the STI technique is optimal for the isolation of SRAM cells because it eliminates planarity concerns and multidimensional oxidation effects, such as the bird's beak formed by the LOCOS isolation techniques, thereby allowing smaller dimensional scaling.

Figure 3 illustrates a cross section of a substrate 30 after a STI step is performed. The STI technique uses trenches 32 etched into the surface of the substrate 30 at the isolation locations, which are subsequently filled with a thermal or deposited oxide. Such trench isolation can provide isolation oxides which extend into the substrate with little or no encroachment.

Flash EPROM and SRAM devices are currently being implemented together within systems and devices. When implemented together, because of the different isolation needs described above, the SRAM device and the flash EPROM are typically manufactured as separate components and then stacked or piggybacked within a package or the system. If the SRAM device and the flash EPROM are implemented separately and piggybacked, then signals sent between the SRAM device and the flash EPROM must exit the originating device and enter the receiving device, leading to possible signal delays. Stacking flash EPROM and SRAM devices within a package may also cause package reliability problems.

Accordingly, what is needed is a method for integrating SRAM and flash EPROM cells within a single device.

SUMMARY OF THE INVENTION

A system for and a method of integrating SRAM cells and flash EPROM cells onto a single silicon substrate includes an area on the silicon substrate where a local oxidation of silicon (LOCOS) isolation technique is implemented and another area on the same silicon substrate where a shallow trench isolation (STI) technique is implemented. Further, this system and method also include flash EPROM cells implemented within the area of the

substrate utilizing the LOCOS isolation technique and SRAM cells implemented within the area of the substrate utilizing the STI technique. Preferably, the LOCOS isolation technique is first implemented to define a flash area of the silicon substrate on which the flash EPROM cell is implemented. Before the LOCOS isolation technique is implemented, an SRAM area is masked. After the LOCOS isolation technique has been fully implemented, the flash area is then preferably masked and the STI technique is implemented in order to define the SRAM area of the silicon substrate on which the SRAM cell is implemented. After the STI technique is implemented, the flash EPROM and the SRAM cells are preferably formed. Thus, the SRAM cells and the flash EPROM cells are both implemented on the common silicon substrate, but yet are appropriately isolated from each other, as well as from other additional devices which may be further implemented on the same silicon substrate, while providing the advantages of respective isolation schemes for the two cells.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a prior art conventional flash EPROM cell.

Figure 2 illustrates a prior art conventional local oxidation of silicon (LOCOS) isolation technique.

Figure 3 illustrates a prior art conventional shallow trench isolation technique.

Figure 4 illustrates a flow chart of the method of manufacturing an SRAM device and a flash EPROM device on the same silicon substrate according to the preferred embodiment of the present invention.

Figure 5 illustrates a substrate having a first STI area and a second LOCOS area on which the SRAM cells and the flash EPROM cells are formed, respectively.

Figure 6 illustrates a step of preparing a substrate as a part of the method of manufacturing according to the present invention.

Figure 7 illustrates a step of masking the STI region and a portion of the LOCOS region as a part of the method of manufacturing according to the present invention.

Figure 8 illustrates a step of etching exposed portions of the LOCOS region as a part of the method of manufacturing according to the present invention.

Figure 9 illustrates a step of growing an oxide field as a part of the method of manufacturing according to the present invention.

Figure 10 illustrates a step of masking the LOCOS region and a portion of the STI region as a part of the method of manufacturing according to the present invention.

Figure 11 illustrates a step of etching exposed portions of the STI region as a part of the method of manufacturing according to the present invention.

Figure 12 illustrates a step of forming shallow trenches within exposed portions of the STI region as a part of the method of manufacturing according to the present invention.

Figure 13 illustrates a step of removing the mask and nitride layer as a part of the method of manufacturing according to the present invention.

Figure 14 illustrates a step of filling the shallow trenches as a part of the method of manufacturing according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A system for and a method of integrating SRAM and flash EPROM cells on a common silicon substrate using appropriate isolation techniques allows the present invention to reduce the package size, increase durability and reliability of the semiconductor device and increase communication speed and accuracy between the SRAM and flash EPROM cells. The present invention allows the STI process and the LOCOS process to be implemented on the same silicon substrate. The STI process is optimized for utilization with the SRAM cells. The STI process allows a greater density of cells to be implemented within an area of the silicon substrate than does the LOCOS process. The LOCOS process is optimized for

utilization with the flash EPROM cells. The LOCOS process is capable of effectively isolating areas in which larger voltages are utilized than the STI process. By implementing the STI process in locations on the common silicon substrate where the SRAM cells are utilized and by implementing the LOCOS process in locations on the common silicon substrate where the flash EPROM cells are utilized, both the SRAM and the flash EPROM cells are each optimally configured on the same silicon substrate.

The present invention maximizes cell density and protection of the cells on the silicon substrate by utilizing a combination of the STI process and the LOCOS isolation process on the same silicon substrate. Further, by utilizing both the SRAM cells and the flash EPROM cells on the common silicon substrate, the present invention is capable of transmitting data between the SRAM cells and the flash EPROM cells faster and more reliably than prior art devices in which the SRAM cells and the flash EPROM cells are implemented on separate devices.

A flow diagram illustrating the steps within the fabrication process of the preferred embodiment of the present invention is illustrated in Figure 4. At the step 300 the substrate is prepared by forming a layer of oxide and nitride on top of the substrate. The substrate is separated into two areas. A first SRAM area is designated for implementation of the SRAM cells. A second flash area is designated for implementation of the flash EPROM cells. Within the first area, the STI process is performed. Within the second area, the LOCOS isolation process is performed.

Before the LOCOS isolation process is performed within the second area, the first area, designated for the STI process, and an active region within the second area are masked, at the step 302. Using this mask step, the first area designated for the STI process is protected from the LOCOS isolation process. Next at the step 304, the layer of nitride is etched from the surface of the substrate in areas not protected by the mask deposited in the step 302. At the step 306, nitride within the second area and the mask covering the first area,

are removed. At the step 308, the LOCOS isolation process is performed, forming a layer of field oxide in the substrate, separated by thin oxide regions, as described above. At the step 310, the second area designated for the LOCOS isolation process and the active regions within the first area, is masked. The second area designated for the LOCOS isolation process is protected from the STI process by this mask. Next, at the step 312, the unmasked areas within the first area, designated for the STI process, are etched to remove the layers of oxide and nitride and a shallow trench is formed within the substrate. Next, at the step 314, the mask over both the second area, designated for the LOCOS isolation process, and the active region within the first area, is then removed. At the step 316, the trenches formed within the substrate are filled. At the step 318, after both the LOCOS isolation process has been performed over the second area and the STI process has been performed over the first area, at least one SRAM cell is implemented in the first area and at least one flash EPROM cell is implemented in the second area, in any appropriate manner known to those skilled in the art. Note that several steps which are known to those skilled in the art, such as channel stop implants, etc., have not been described herein, in order to highlight the major process steps within the method of the present invention and the differences between the present invention and the prior art.

The method of the present invention preferably performs the LOCOS isolation process first on a portion of the common silicon substrate while protecting other areas of the silicon substrate, designated for the STI process. After the LOCOS process is completed, the STI process is preferably performed on a different portion of the common silicon substrate while protecting other areas of the silicon substrate, designated for the LOCOS isolation process. After the STI process is completed, the present invention then implements the SRAM and the flash EPROM cells within areas of the common silicon substrate utilizing the STI process and the LOCOS isolation process, respectively. In a first alternate embodiment, the STI process is performed before the LOCOS isolation process. In a second alternate embodiment, the

implementation of the SRAM cells and the flash EPROM cells occur after completion of each of the STI process and the LOCOS isolation process, respectively.

Figures 5-14 illustrate cross sectional views of the various steps in the process of the preferred embodiment of the present invention, as set forth in Figure 4. The process begins on a substrate, as illustrated in Figure 5. The substrate 100 includes a first area 102, designated for the STI process, and a second area 104, designated for the LOCOS isolation process. The SRAM devices are preferably implemented in this first area 102 after the STI process has been performed. Within the Figures 5-14, the first area 102 and the second area 104 are shown separated by the vertical dashed line 150. It should be understood that the vertical dashed line 150 is provided for clarity in the illustration of the apparatus and method of the present invention, but in practice, the substrate 100 is a single uniform substrate. The flash EPROM devices are preferably implemented in the second area 104 after the LOCOS isolation process has been performed. The substrate 100 is prepared to accept both the STI and LOCOS isolation techniques by depositing an oxide layer 110 and a nitride layer 120, over the substrate 100, as illustrated in Figure 6. The nitride layer 120 preferably protects the underlying substrate 100 and the layer of oxide 110 from steps performed for the STI process and the LOCOS process. More specifically, the areas covered by the layer of nitride 110 will not react and will not oxidize during the steps of the STI process and the LOCOS process. The oxide layer 110 functions as a sacrificial layer and is preferably utilized as a base surface on which to grow oxide fields.

In the preferred embodiment, the LOCOS isolation process is implemented on the substrate 100 before the STI process. Before the LOCOS isolation process is performed, a mask 130 is formed over the first area 102, designated for the STI process, and an active region within the second area 104, as illustrated in Figure 7. The mask 130 is preferably formed from a photoresist.

As shown in Figure 8, the layer of nitride 120 is preferably etched away in areas not covered by the mask 130. The mask 130, covering the first area and the active area within the second area, is then removed. Next, as shown in Figure 9, the LOCOS isolation process is performed over the unmasked portions, forming field oxide layers 200. The field oxide layers 200 are preferably between 4000 and 6500 angstroms in thickness in order to appropriately isolate connection lines and memory cells.

Preferably after the LOCOS isolation process is completed, the STI process commences by forming a mask 170 over the second area 104 and an active region within the first area 102, as illustrated in Figure 10. The mask 170 is preferably formed from a photoresist. The mask 170 protects the second area 104 and the active region within the first area 102 from any of the steps involved in the STI process.

Next, as shown in Figure 11, the layer of nitride 120 and the layer of oxide 110 are preferably etched away in the STI areas which are not covered by the mask 170. Following the step of etching away the layer of nitride 120 and the layer of oxide 110, the exposed silicon substrate 100 is etched away to form shallow trenches 220, as shown in Figure 12. The mask 170 and the underlying layer of nitride 120 are removed, as illustrated in Figure 13.

The shallow trenches 220 are then preferably filled with an insulating oxide substance 225 and a blanket etch is performed, as shown in Figure 14, to expose the active regions 210 and 230. The insulating oxide substance 225 provides an insulating property which electrically isolates the area 220 on the substrate 100 from other areas on the substrate 100. The active region 210 corresponds to the location for implementing semiconductor devices, preferably flash EPROM devices, which are isolated by the LOCOS process. The active region 230 corresponds to the location for implementing semiconductor devices, preferably SRAM devices, which are isolated by the STI process.

Preferably, SRAM cells are then implemented within the active regions 230 of the first area in any appropriate manner known to those skilled in the art. Similarly, flash EPROM cells are preferably implemented within the active regions 210 of the second area in any appropriate manner known to those skilled in the art.

In the preferred embodiment of the present invention, the LOCOS isolation process is implemented on the silicon substrate before the STI process. Further, both the STI process and the LOCOS isolation process are completed on the silicon substrate prior to implementation of either the SRAM cells or the flash EPROM cells on the silicon substrate. In a first alternate embodiment, the STI process is implemented on the silicon substrate prior to the LOCOS isolation process. In a second alternate embodiment, the corresponding semiconductor devices are implemented immediately after each of the respective isolation techniques are implemented on the silicon substrate. For example, in the second alternate embodiment, the SRAM cells are implemented on the silicon substrate after the STI process is implemented and before the LOCOS isolation process is implemented. The STI process and the LOCOS isolation process are utilized in the preferred embodiment of the present invention and correspond with the SRAM and flash EPROM cells, respectively. However, as should be apparent to those skilled in the art, various different isolation techniques along with a variety of different semiconductor devices are capable of being utilized.

The present invention integrates SRAM and flash EPROM cells on a common silicon substrate using different isolation techniques for the SRAM and flash EPROM cells. By utilizing the STI isolation technique for the SRAM cells and the LOCOS isolation technique for the flash EPROM cells on the common silicon substrate, the present invention combines the SRAM and flash EPROM cells on the same substrate, using the respective optimal isolation techniques. By utilizing the optimal isolation technique for each type of cell on the common substrate, the package size of the substrate is minimized and the reliability of the cells within the substrate is increased. In addition, by implementing both the SRAM and

flash EPROM cells on a common silicon substrate, there is less interference and quicker transmission of data between the SRAM and flash EPROM cells, compared to prior art devices in which the SRAM cells and the flash EPROM cells are implemented on separate devices.

The present invention has been described in terms of specific embodiments incorporating details to facilitate the understanding of principles of construction and operation of the invention. Such reference herein to specific embodiments and details thereof is not intended to limit the scope of the claims appended hereto. It will be apparent to those skilled in the art that modifications may be made in the embodiment chosen for illustration without departing from the spirit and scope of the invention.

CLAIMS

I claim:

1. A semiconductor device comprising:
a common substrate;
an SRAM device implemented on the common substrate and isolated by a first isolation technique; and
a flash EPROM device implemented on the common substrate and isolated by a second isolation technique.

2. The semiconductor device according to claim 1 wherein the first isolation technique is an STI technique.

3. The semiconductor device according to claim 1 wherein the second isolation technique is a LOCOS isolation technique.

4. The semiconductor device according to claim 1 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

5. A system for allowing different types of isolation techniques during fabrication of a semiconductor device, comprising:
a common substrate having a first portion on which a first isolation technique is implemented during processing and a second portion on which a second isolation technique is implemented during processing;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

6. The system according to claim 5 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

7. The system according to claim 5 wherein the first isolation technique is an STI technique.

8. The system according to claim 5 wherein the second isolation technique is a LOCOS technique.

9. A semiconductor device comprising:

a common substrate having a first portion on which an STI isolation technique is implemented during processing and a second portion on which a LOCOS isolation technique is implemented during processing;

an SRAM device implemented on the first portion of the substrate; and

a flash EPROM device implemented on the second portion of the substrate.

10. The semiconductor device according to claim 9 wherein the SRAM device is coupled to the flash EPROM device for transmitting signals between the SRAM device and the flash EPROM device.

11. A method of integrating two types of isolation techniques on a single substrate during fabrication of a semiconductor device, comprising the steps of:

implementing a LOCOS isolation technique in a LOCOS area on the substrate;

implementing a first semiconductor device in the LOCOS area on the substrate;

implementing an STI technique in an STI area on the substrate; and

implementing a second semiconductor device in the STI area on the substrate.

12. The method according to claim 11 further comprising the step of masking the LOCOS area when the step of implementing the STI technique is performed.

13. The method according to claim 11 further comprising the step of masking the STI area when the step of implementing the LOCOS technique is performed.

14. The method according to claim 11 wherein the first semiconductor device is a flash EPROM device, and the second semiconductor device is an SRAM device.

15. A method of fabricating a semiconductor device including both an SRAM device and a flash EPROM device, comprising the steps of:

implementing a LOCOS isolation technique in a LOCOS area on the substrate;

implementing the flash EPROM device in the LOCOS area on the substrate;

implementing an STI technique in an STI area on the substrate; and

implementing the SRAM device in the STI area on the substrate.

16. The method according to claim 15 further comprising the step of masking the LOCOS area when the step of implementing the STI technique is performed.

17. The method according to claim 15 further comprising the step of masking the STI area when the step of implementing the LOCOS technique is performed.

ABSTRACT

A system for and a method of integrating SRAM cells and flash EPROM cells onto a single silicon substrate includes an area on the silicon substrate where a local oxidation of silicon (LOCOS) isolation technique is implemented and another area on the same silicon substrate where a shallow trench isolation (STI) technique is implemented. Further, this system and method also include flash EPROM cells implemented within the area of the substrate utilizing the LOCOS isolation technique and SRAM cells implemented within the area of the substrate utilizing the STI technique. Preferably, the LOCOS isolation technique is first implemented to define a flash area of the silicon substrate on which the flash EPROM cell is implemented. Before the LOCOS isolation technique is implemented, an SRAM area is masked. After the LOCOS isolation technique has been fully implemented, the flash area is then preferably masked and the STI technique is implemented in order to define the SRAM area of the silicon substrate on which the SRAM cell is implemented. After the STI technique is implemented, the flash EPROM and the SRAM cells are preferably formed. Thus, the SRAM cells and the flash EPROM cells are both implemented on the common silicon substrate, but yet are appropriately isolated from each other, as well as from other additional devices which may be further implemented on the same silicon substrate, while providing the advantages of respective isolation schemes for the two cells.

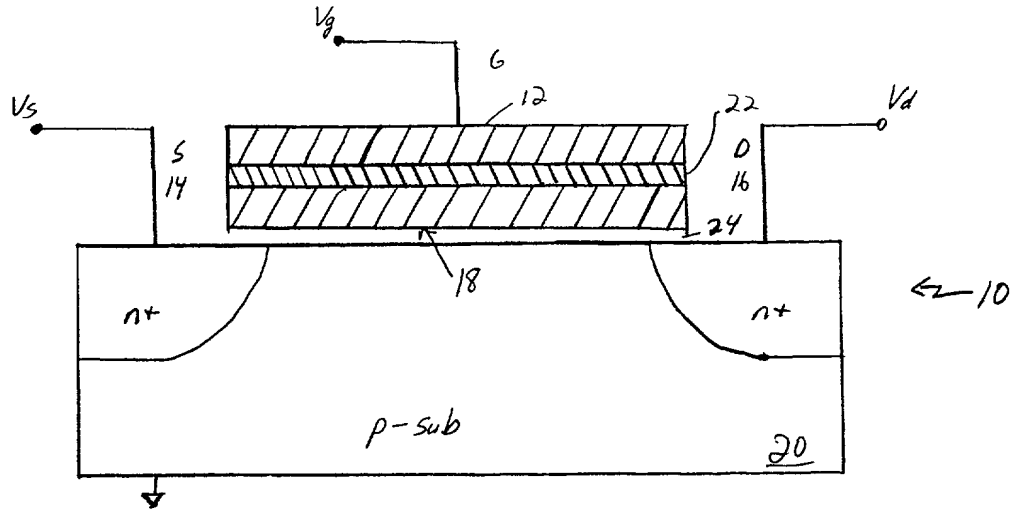


FIGURE 1
(PRIOR ART)

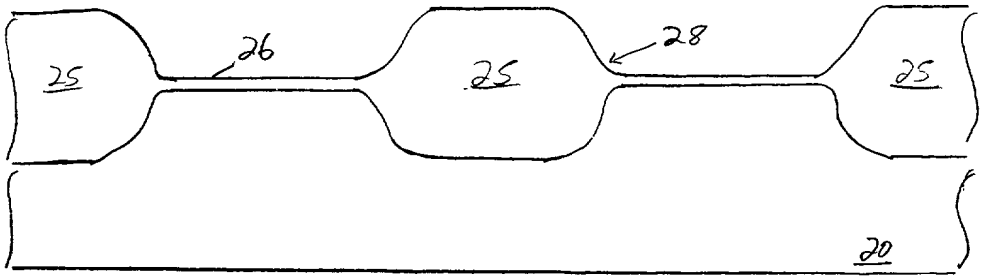


FIGURE 2
(PRIOR ART)

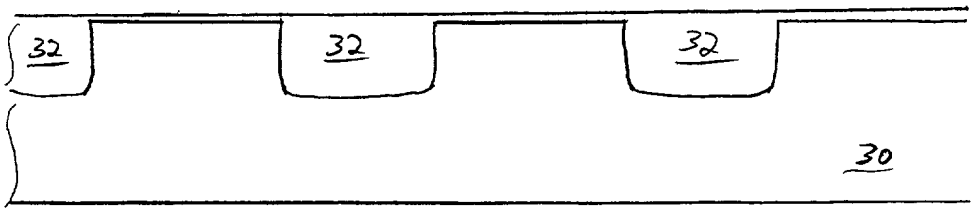


FIGURE 3
(PRIOR ART)

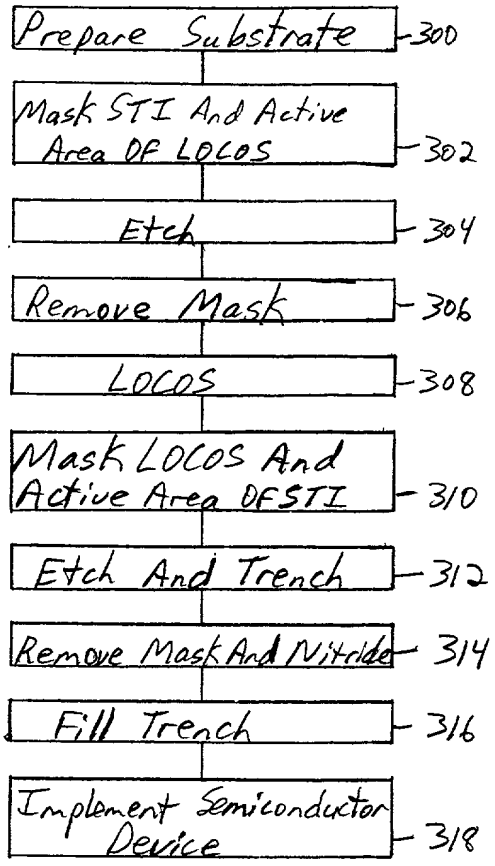

Prepare Substrate
300
Mask STI And Active Area Of LOCOS
302
Etch
304
Remove Mask
306
LOCOS
308
Mask LOCOS And Active Area OFSTI
310
Etch And Trench
312
Remove Mask And Nitride
314
Fill Trench
316
Implement Semiconductor Device
318

FIGURE 4

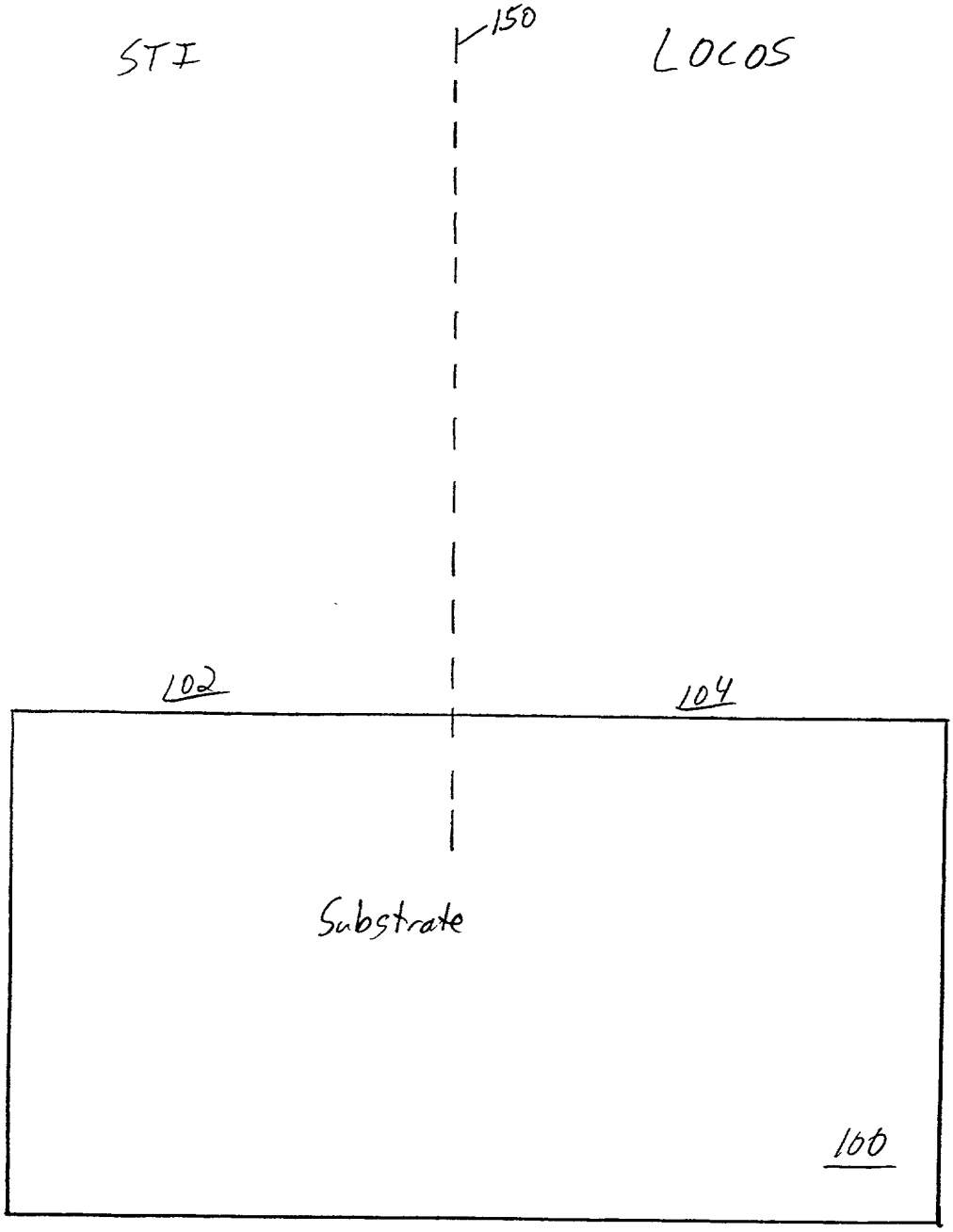


FIGURE 5

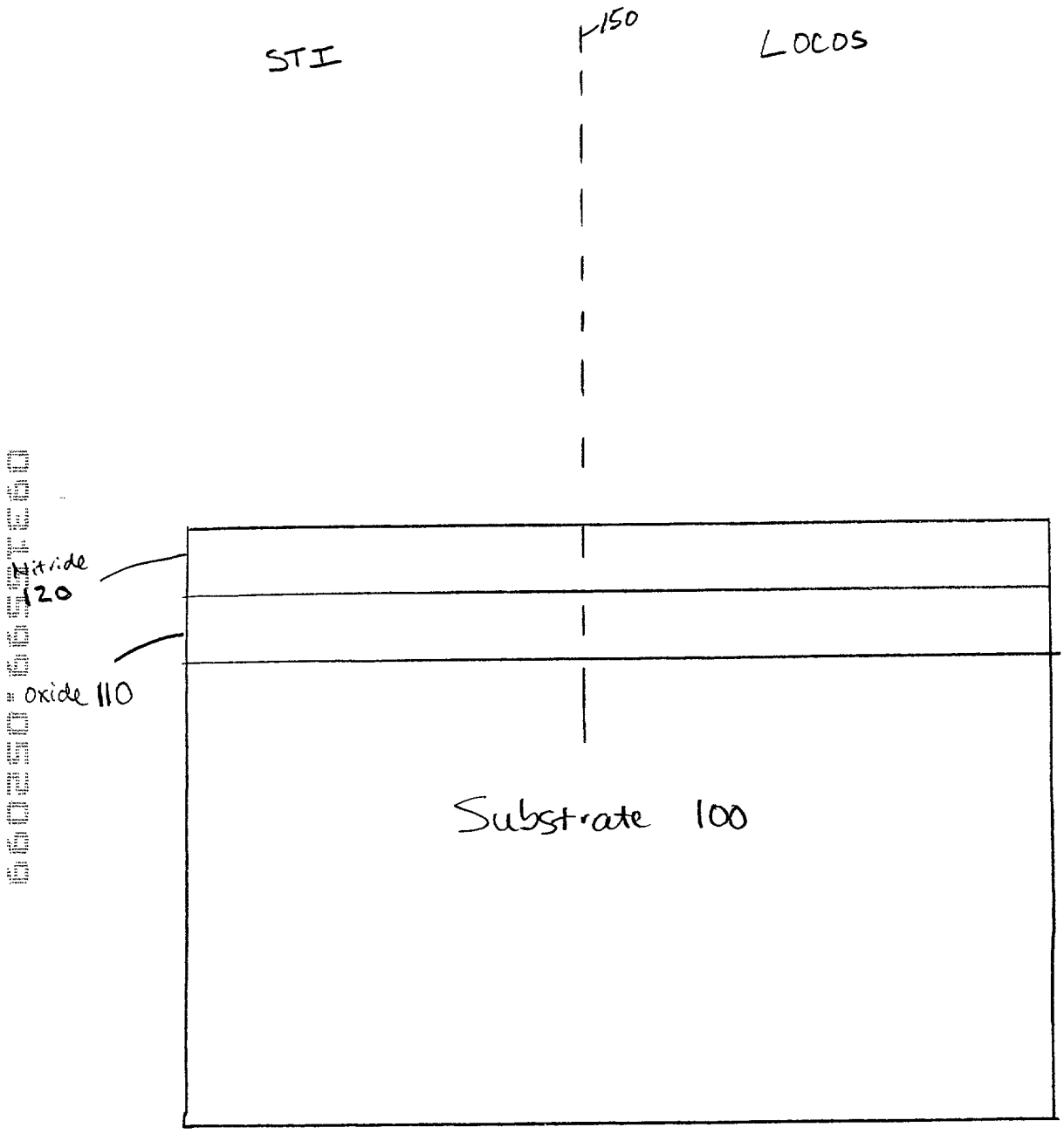


FIGURE 6

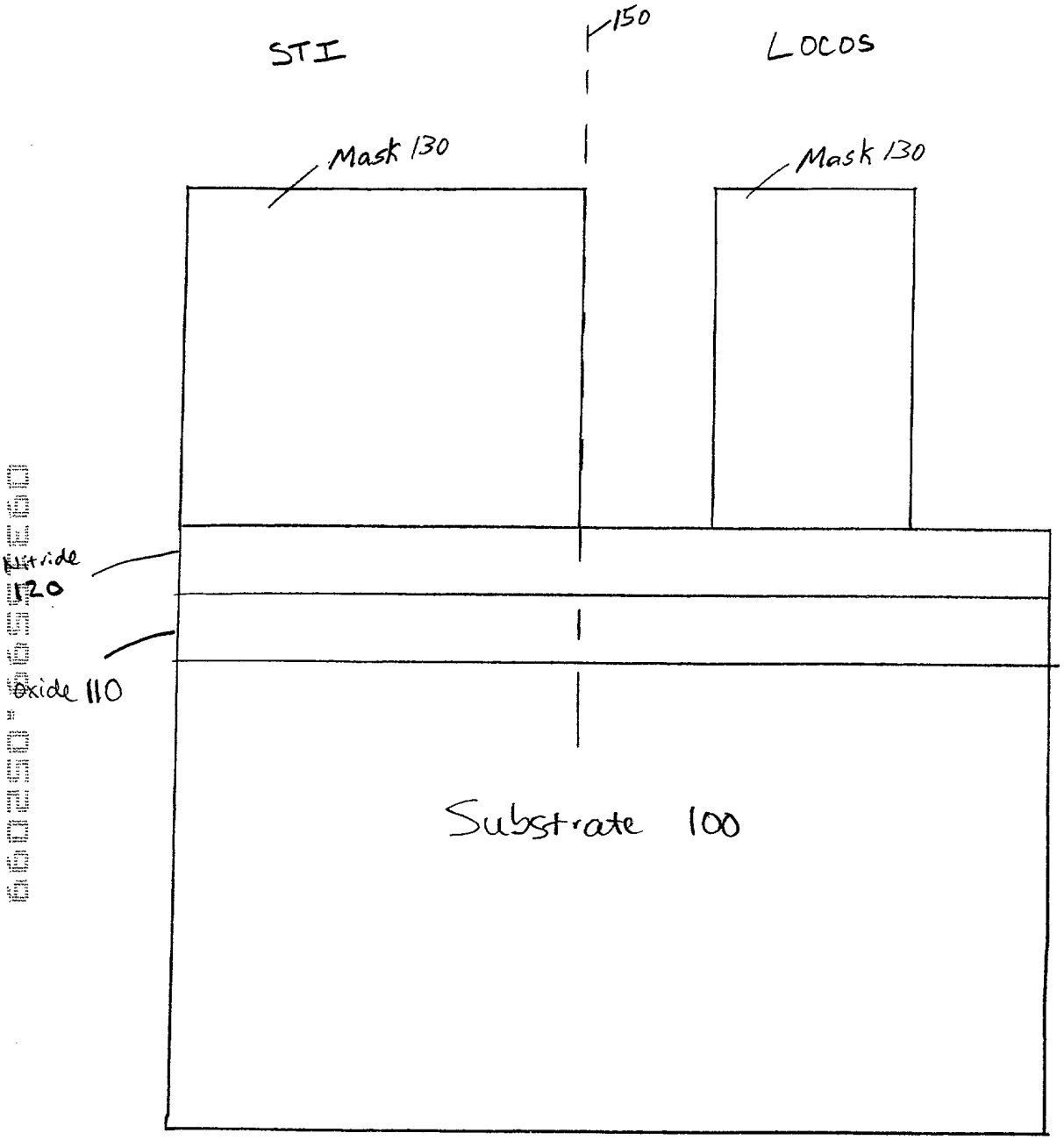

STI
150
LOCOS
Mask 130
Mask 130
Nitride 120
Oxide 110
Substrate 100

FIGURE 7

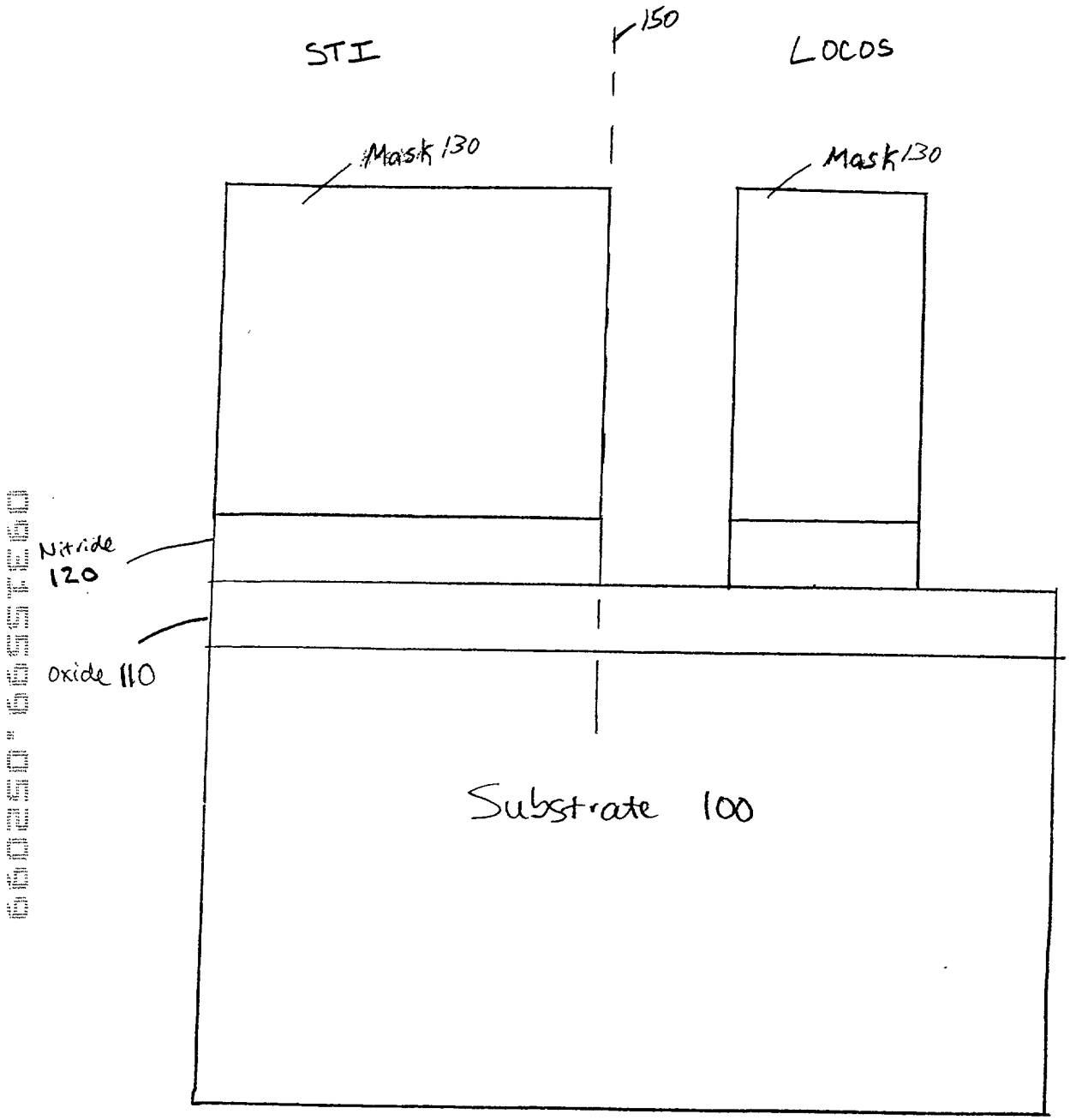

STI
150
LOCOS
Mask 130
Mask 130
Nitride 120
oxide 110
Substrate 100

FIGURE 8

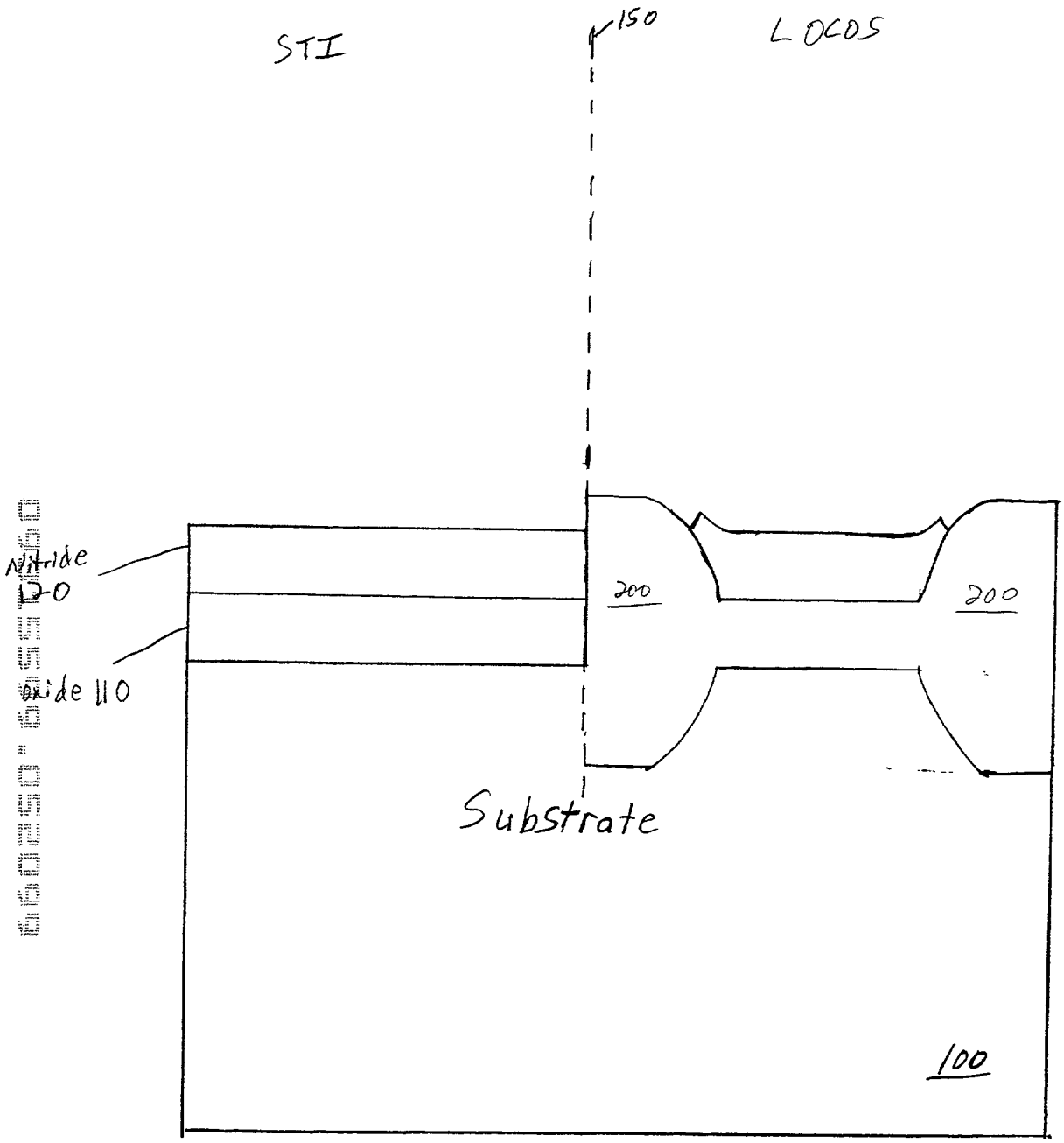


FIGURE 9

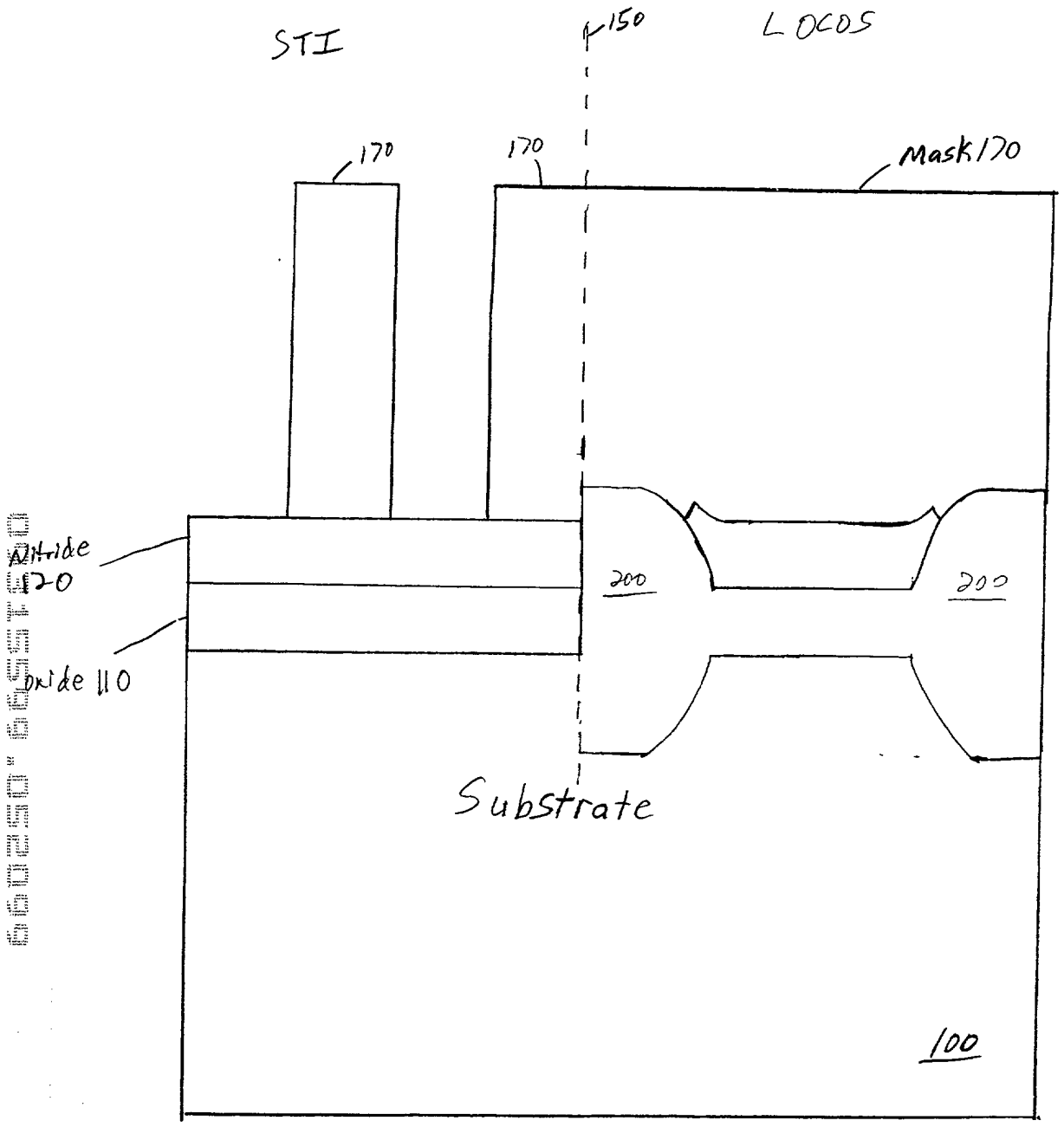

STI
150
LOCOS
170
170
Mask 170
Nitride 120
Oxide 110
200
200
Substrate
100

FIGURE 10

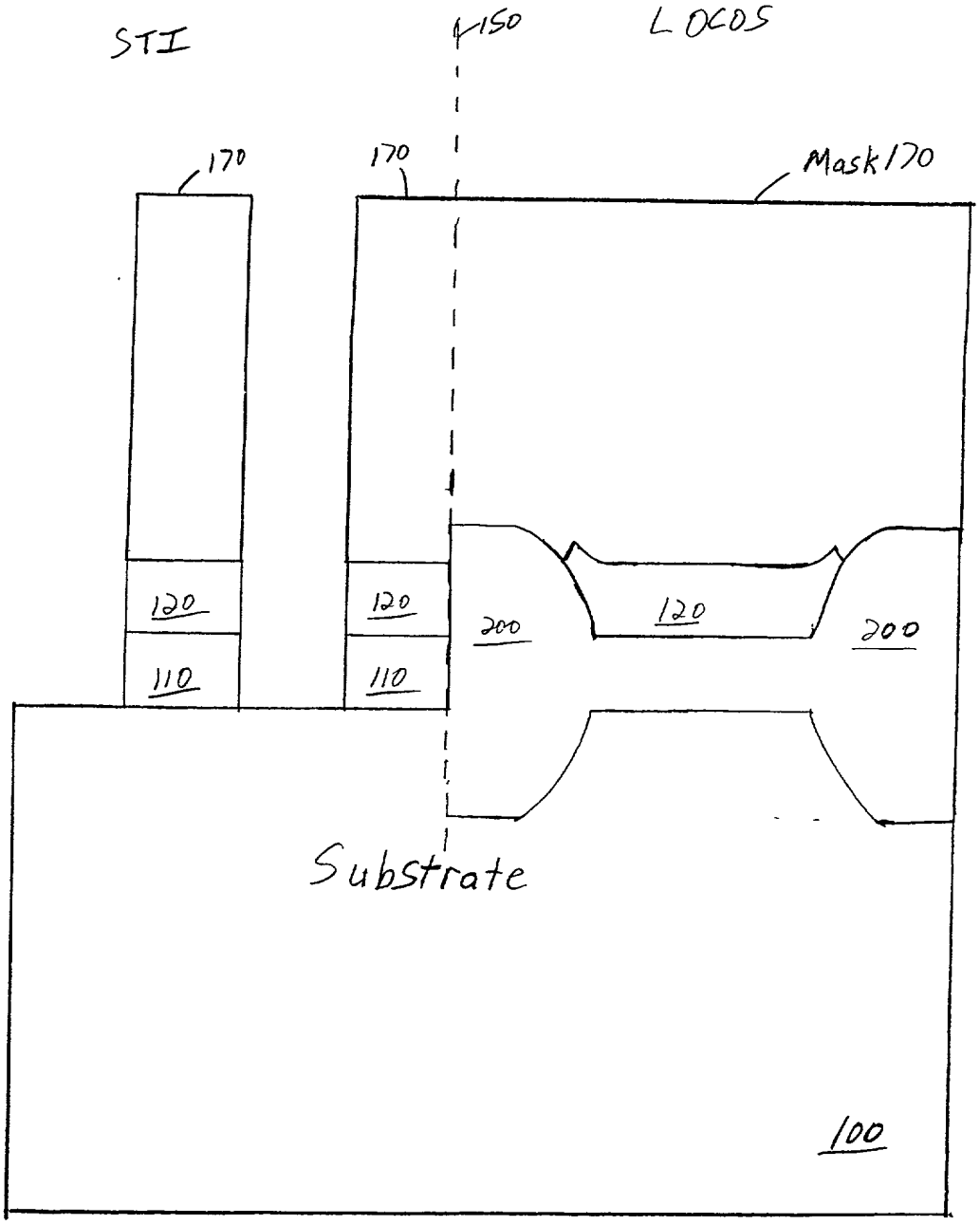

STI
150
LOCOS
170
170
Mask 170
120
120
200
120
200
110
110
Substrate
100

FIGURE 11

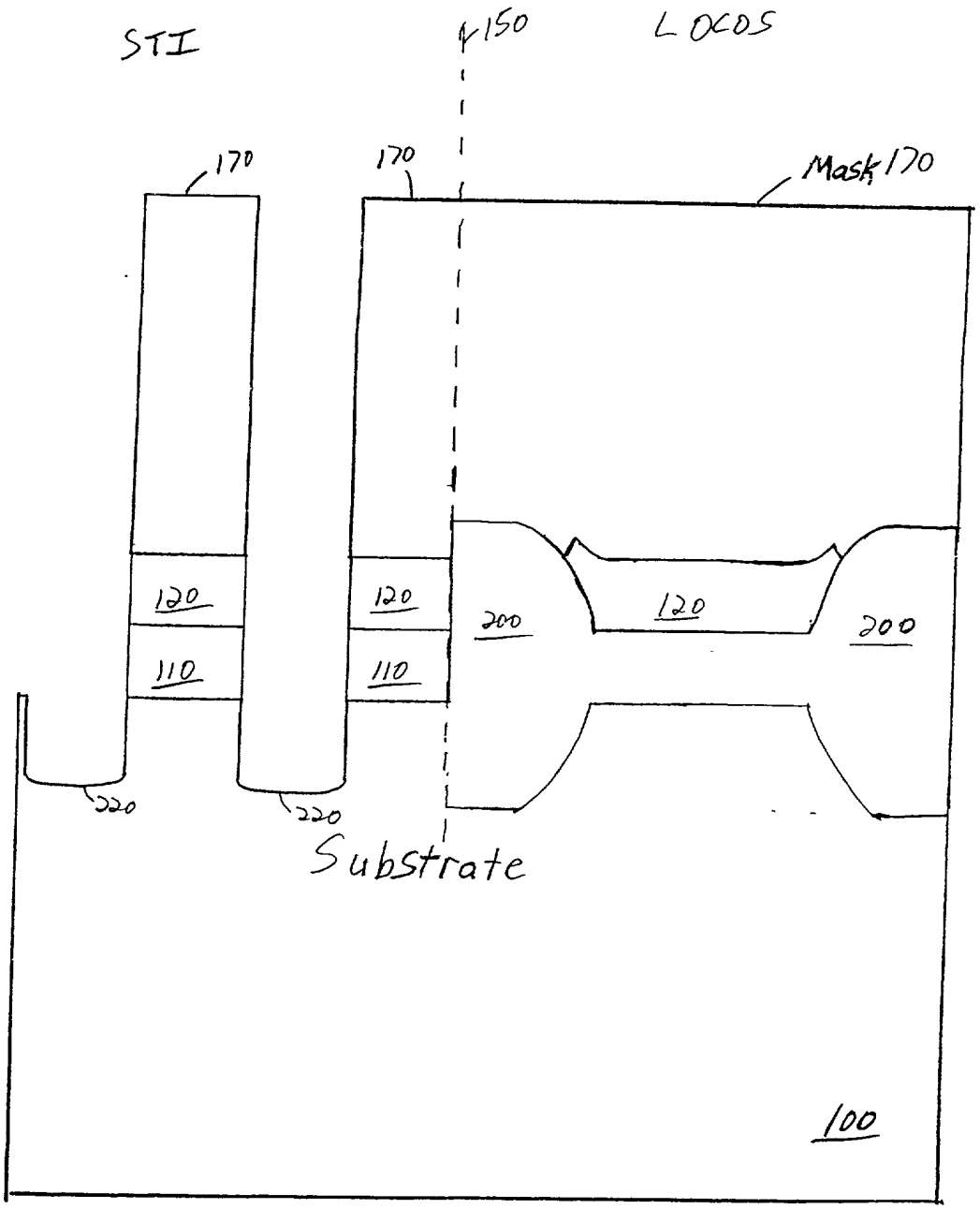

STI
150
LOCOS
170
170
Mask 170
120
120
120
110
110
200
200
220
220
Substrate
100

FIGURE 12

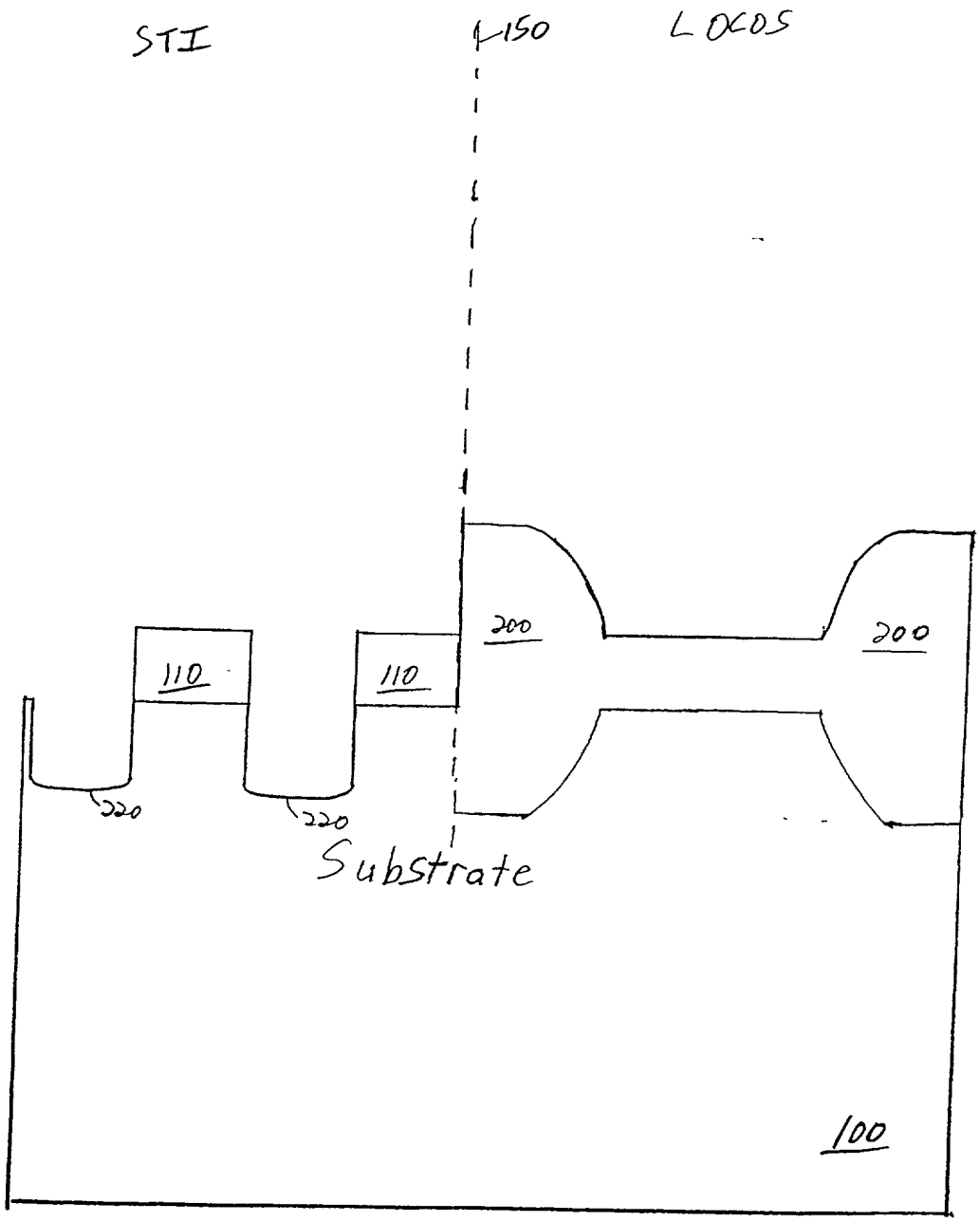


FIGURE 13

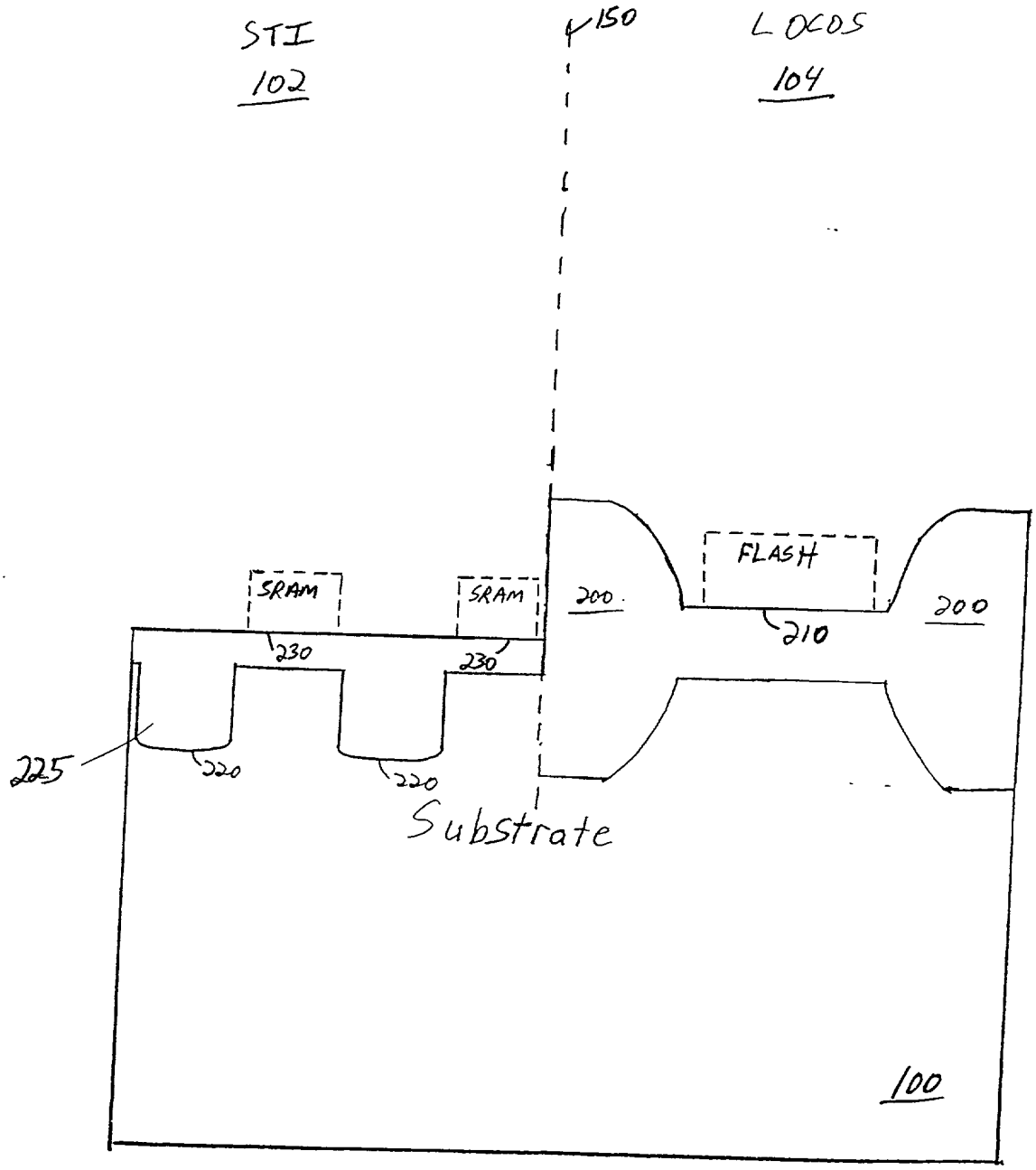

STI
102
150
LOCOS
104
SRAM
SRAM
200
FLASH
200
230
230
210
225
220
220
Substrate
100

FIGURE 14

Express Mail Label No. EL191268477US

PATENT
Attorney Docket No.: ALSC-00300

DECLARATION FOR PATENT APPLICATION

As the below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name. I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **A METHOD OF AND APPARATUS FOR INTEGRATING FLASH EPROM AND SRAM CELLS ON A COMMON SUBSTRATE**. The specification of which is attached hereto. I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, Section 1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

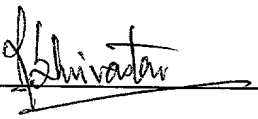
Prior Foreign Application(s)			Priority Claim	
			Yes	No
Number	Country	Day/Month/Year Filed		

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application Serial No.	Filing Date	Status: Patented, Pending, Abandoned

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole and First Inventor: Ritu Shrivastava

Inventor's Signature:  5/19/99
Date

Residence: 44455 Parkmeadow Drive, Fremont, California 94539
Citizenship: United States
Post Office Address: 44455 Parkmeadow Drive, Fremont, California 94539

Express Mail Label No. EL191268477US

PATENT
Attorney Docket No.: ALSC-00300

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	Group:
	)	Art Unit:
Ritu Shrivastava	)	Examiner:
	)	
Serial No.:	)	
	)	
Filed: herewith	)	**POWER OF ATTORNEY BY ASSIGNEE**
	)	
For: **A METHOD OF AND APPARATUS FOR INTEGRATING FLASH EPROM AND SRAM CELLS ON A COMMON SUBSTRATE**	)	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Alliance Semiconductor, Assignee of the above-identified application by Assignment dated _____ hereby appoints the members of the firm of HAVERSTOCK & OWENS LLP, a firm including Thomas B. Haverstock (Reg. No. 32,571), Jonathan O. Owens (Reg. No. 37,902), Derek J. Westberg (Reg. No. 40,872) and Richard H. Butt (Reg. No. 40,932), 260 Sheridan Avenue, Suite 420, Palo Alto, California 94306, telephone: (650) 833-0160, facsimile: (650) 833-0170, as its attorneys with full power of substitution to prosecute this application and to transact all business in the Patent and Trademark Office in connection therewith.

Please direct all correspondence regarding this application to the following:

Jonathan O. Owens
HAVERSTOCK & OWENS LLP
260 Sheridan Avenue, Suite 420
Palo Alto, California 94306
Telephone: (650) 833-0160
Facsimile: (650) 833-0170

I hereby certify that the Assignment document filed with the application or filed subsequent to the filing date of the application, has been reviewed and I hereby certify that, to the best of my knowledge and belief, title is with **Alliance Semiconductor**.

Alliance Semiconductor

Dated: 5/18/99

By: N D Reddy
Name: N. Damodar Reddy
Title: President